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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 18

Application Number: 09/544,054
Filing Date: April 06, 2000
Appellant(s): YONA ET AL.

Joseph B. Ryan (Reg. No. 37,922)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on 21st of July, 2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 1-11, 13-29 and 31-38 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

Applicant's Admitted Prior Art

5,734,656	Prince et al.	3-1998
WO 93/15464	Porter et al.	8-1993
5,771,358	LaBerge	6-1998
5,838,681	Bonomi et al.	11-1998
6,016,528	Jaramillo et al.	1-2000
2001/0043700	Shima et al.	3-1999
6,400,819	Nakano et al.	6-2002
6,219,706	Fan et al.	4-2001
5,768,270	Ha-Duong	6-1998
5,875,351	Riley	2-1999

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Prince et al. [US 5,734,656 A; hereinafter Prince].

Referring to claim 1, Prince discloses a modular switch (i.e., network hub 200 of Fig. 2), comprising: a plurality of backplane sub-buses (i.e., cell slots in Fig. 7; i.e. time dimension multiplexing buses of ATM switching backplane bus; See col. 7, lines 33-37); a plurality of cards (i.e., LAN modules 201-204 and ATM module 206 of Fig. 2) which are each allocated one or more of said backplane sub-buses (See col. 12, lines 36-40); and a controller (i.e., master control processor[MCP] 430 of Fig. 4) which dynamically allocates said backplane sub-buses to said plurality of cards, based on bandwidth needs of said cards (See col. 12, lines 32-35 and col. 13, lines 41-46).

Referring to claim 2, Prince discloses a bandwidth capacity (i.e. full bandwidth of ATM switching core 370 in Fig. 3) of substantially all said backplane sub-buses is less than said sum of a maximal transmission bandwidth capacity of said cards (See col. 5, lines 41-47 and col. 9, lines 4-8; i.e. wherein the fact that the full bandwidth of the ATM switch is thought of as being available to all devices attached to the network implies that the sum of bandwidth capacities of network devices is greater than the full bandwidth of the ATM switching core).

Referring to claim 3, Prince discloses said controller (i.e., MCP 430 of Fig. 4) is implemented by one (i.e., LAN module 401 of Fig. 4) of said cards (i.e., LAN modules 401,412 of Fig. 4; See col. 12, lines 46-49).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Prince [US 5,734,656 A].

Referring to claim 4, Prince discloses 1) said controller is implemented by one of said cards (See above claim 3 rejection.) and 2) said controller (i.e., MCP 430 of Fig. 4) may reside on any LAN or ATM module coupled to the switch fabric without having any affect on the functionality of the device (See col. 12, lines 49-53). It is unclear whether Prince disclose one or more said cards have said controllers and one of said cards is selected dynamically. The examiner takes official notice that said dynamic selection feature in said switch among said controllers in said two or more modules is well known in the art of fault tolerant computing system. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included 1) said controllers in said two or more modules, and 2) said dynamic selection feature in said switch for the advantage of a fault tolerance capability based on said redundant controllers on said two or more modules.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Prince [US 5,734,656 A] in view of Bonomi et al. [US 5,838,681 A; hereinafter Bonomi].

Referring to claim 5, Prince discloses all the limitations of claim 5 except that does not teach said cards transmit messages which indicate their bandwidth needs to said controller. Bonomi discloses a

dynamic allocation of port bandwidth, including cards (i.e., adaptors 100 of Fig. 4) transmit messages (See col. 9, line 29) which indicate their bandwidth needs (i.e. an explicit request for bandwidth; See col. 9, line 25) to a controller (i.e., CPU 96 of Fig. 4). Refer to col. 9, lines 24-30. Therefore, it would have been obvious one of ordinary skill in the art at the time the invention was made to have included said dynamic allocation of port bandwidth, as disclosed by Bonomi, in said switch, as disclosed by Prince, for the advantage of allowing a bandwidth allocation based on the particular type of data awaiting transfer (See Bonomi, col. 9, lines 16-24).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Prince [USPN 5,734,656 A] in view of Jaramillo et al. [US 6,016,528 A; hereinafter Jaramillo].

Referring to claim 6, Prince discloses all the limitations of claim 6 except that does not teach each of said cards in said switch has a priority value which indicates its entitlement to bandwidth. Jaramillo discloses a priority arbitration system, wherein each of cards (i.e., device 0-5 in Fig. 3) has a priority value which indicates its entitlement to bandwidth (See col. 5, lines 23-34) and a controller (i.e., PCI arbiter 508 of Fig. 5) allocates backplane (i.e., PCI bus) sub-buses (i.e., ownership of PCI bus cycles) based on said priority values (i.e., device priorities) of said cards (i.e., PCI agents 501-507 of Fig. 5). Refer to col. 5, lines 35+. Therefore, it would have been obvious one of ordinary skill in the art at the time the invention was made to have included said priority arbitration system, as disclosed by Jaramillo, in said controller of said switch, as disclosed by Prince, for the advantage of providing predictable latency and guaranteed access for said cards coupled to said backplane sub-buses, and providing an arbitration process which is much more flexible with regard to allocating bus bandwidth (See Jaramillo, col. 8, lines 38-42).

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prince [USPN 5,734,656 A] in view of Applicant's Admitted Prior Art [hereinafter AAPA].

Referring to claims 7 and 8, Prince discloses all the limitations of claims 7 and 8, respectively, except that does not disclose 1) all said backplane sub-buses have said same bandwidth capacity, and 2) said plurality of backplane sub-buses comprise at least two sub-buses with different bandwidths. AAPA teaches all backplane sub-buses (i.e., cell slots) in a switch (i.e., modular switch) have a same bandwidth capacity (See page 1, lines 16-18), and said plurality of backplane sub-buses (i.e., cell slots) in a switch (i.e., modular switch) comprise at least two sub-buses with different bandwidths (i.e., some large bus portions and other smaller bus portions; See page 1, lines 20-21). Therefore, it would have been obvious one of ordinary skill in the art at the time the invention was made to have applied said various method of bandwidth allocation, as disclosed by AAPA, to said switch, as disclosed by Prince, so as to allow said cards to use said sub-buses efficiently using said various method of bandwidth allocation (See AAPA, page 1, lines 9-15).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Prince [US 5,734,656 A] in view of Shima et al. [US 2001/0043700 A1; hereinafter Shima].

Referring to claim 9, Prince disclose all the limitations of claims 9 except that does not disclose said controller confiscates one or more sub-buses from one or more of cards when said one or more sub-buses are more needed by one or more other cards. Shima discloses a bandwidth allocation method (See Fig. 8), wherein a controller (i.e., peripheral device 230 of Fig. 2) confiscates one or more sub-buses (i.e., bandwidth) from one or more of cards (i.e., devices in multimedia network 100 of Fig. 1) when said one or more sub-buses are more needed by one or more other cards (See paragraph [0045], lines 1-7 on page 4). Therefore, it would have been obvious one of ordinary skill in the art at the time the invention was made to have applied said bandwidth allocation method, as disclosed by Shima, to said controller of said switch, as disclosed by Prince, for the advantage of providing for dynamic reallocation of said bandwidth (See Shima, paragraph [0045], lines 13-14 on page 4).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Prince [USPN 5,734,656 A] in view of Shima [US 2001/0043700 A1] as applied to claim 9 above, and further in view of Nakano et al. [US 6,400,819 B1; hereinafter Nakano].

Referring to claim 10, Prince, as modified by Shima, discloses all the limitations of claims 10 including said bandwidth release stage, whereafter said controller allocates a confiscated sub-bus to a card (See Shima, paragraph [0045], lines 8-13 on page 4) except that does not disclose said allocation should be processed after receiving confirmation from said card from which said sub-bus was confiscated that said sub-bus was freed from its allocation. Nakano discloses a bandwidth release module (See Fig. 17) , wherein a sub-bus (i.e., bandwidth) releasing stage includes a receiving confirmation (i.e., box 1704; wait for acknowledgement packet) from a card (i.e., release requestor) from which said sub-bus was confiscated that said sub-bus was freed from its allocation (See col. 13, lines 53-65). Therefore, it would have been obvious one of ordinary skill in the art at the time the invention was made to have included said bandwidth release module, as disclosed by Nakano, in said controller of said switch, as disclosed by Prince, as modified by Shima, for the advantage of providing an interface for accepting said bandwidth release with said receiving confirmation (See Nakano, col. 14, lines 5-6 and Fig. 17) before said dynamic reallocation of said bandwidth (See Shima, paragraph [0045], lines 13-14 on page 4).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Prince [US 5,734,656 A] in view of LaBerge [US 5,771,358 A].

Referring to claim 11, Prince discloses all the limitations of claim 11 except that does not disclose said controller calculates, for each of said cards, a bus demand value which represents an entitlement and need of said card to receive a sub-bus. LaBerge discloses a method for apportioning computer bus bandwidth, wherein a controller (i.e., bus controller 24 of Fig. 1) calculates, for each of said cards (i.e., bus requesters 26,28,30,32 of Fig. 1), a bus demand value (i.e., weighting value) which represents an entitlement and need of said card to receive a sub-bus (See col. 3, lines 33-36), and said controller

allocates free sub-buses which are not allocated to said cards with the highest bus demand values (See col.4, lines 30-32 and lines 37-40). Therefore, it would have been obvious one of ordinary skill in the art at the time the invention was made to have applied said bandwidth allocation method, as disclosed by LaBerge, to said controller of said switch, as disclosed by Prince, for the advantage of apportioning said bandwidth based on said bus demand value enables higher bandwidth cards to continue to operate at a relatively high bandwidth when said bus is saturated (See LaBerge, col. 6, lines 19-21).

Claims 13, 14 and 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Porter et al. [WO 93/15464; cited by applicant; hereafter Porter].

Referring to claim 13, Porter discloses a modular switch (i.e., backplane 20 with line switches in Fig 2), comprising: a plurality of backplane sub-buses (i.e., 'N' switched lines of Fig 3; See page 7, lines 19-23 and page 14, lines 20-23); and a plurality of cards (i.e., boards; See page 1, lines 9-10 and page 3, lines 21+) which are configurable to listen to a variable number of said backplane sub-buses (See page 4, lines 2-9 and page 15, line 25 through page 16, line 2).

Referring to claim 14, Porter discloses at least one of said plurality of cards listens to fewer than all the backplane sub-buses (See page 3, line 21 through page 4, line 6).

Referring to claim 16, Porter discloses each of said cards is configured to listen (i.e., communicate) to a respective group (i.e., cluster) of peer cards (i.e., a group of cards which have a particular aspect of the operation). Refer to page 4, lines 2-6 and page 8, line 19.

Referring to claim 17, Porter discloses said sub-buses to which each of said plurality of cards listens are said sub-buses to which said respective group of peer cards transmit (See page 4, lines 2-6; i.e., wherein in fact that board in a cluster communicates with other boards in the cluster anticipates that an 'N' channel (i.e., sub-buses) to which each of said plurality of boards (i.e., a group of boards in a cluster) listens (i.e., communicate) is said 'N' channel (i.e., sub-buses) to which said respective group of peer cards (i.e., said group of boards in said cluster) communicate (i.e. transmit)).

Referring to claim 18, Porter discloses each card (i.e., board) listens to said cards which listen to it (i.e., because of communicating each other in a cluster of cards; See page 4, lines 2-6).

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Porter [WO 93/15464] in view of LaBerge [US 5,771,358 A].

Referring to claim 15, Porter discloses all the limitations of claim 15 except that does not teach a controller which dynamically changes said sub-buses to which each card listens. LaBerge discloses a controller (i.e., bus controller 24 of Fig. 1) which dynamically changes (See col. 2, lines 23-29) said sub-buses to which each card listens (See col. 5, lines 9+). Therefore, it would have been obvious one of ordinary skill in the art at the time the invention was made to have included said dynamic embodiment of said controller, as disclosed by LaBerge, in said modular switch, as disclosed by Porter, for the advantage of enabling higher bandwidth cards to continue to operate at a relatively high bandwidth when said backplane sub-bus is saturated (See LaBerge, col. 6, lines 19-21).

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Porter [WO 93/15464].

Referring to claim 19, Porter discloses all the limitations of claim 19 except that does not teach at least one card listens to fewer than all said cards that listen to it. The examiner takes official notice that said configuration (i.e., few-to-many work group environment) is well known in the art of work group environment setting with access privileges in network. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to recognize said at least one card listens to fewer than all said cards that listen to it via said work group environment setting with access privileges since it would have allowed for greater security in said work group.

Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Porter [WO 93/15464] in view of Fan et al. [US 6,219,706 B1; hereinafter Fan].

Referring to claims 20 and 21, Porter discloses all the limitations of claims 20 and 21, respectively, except that does not teach 1) said peer group of one or more cards changes as a function of

time, and 2) said peer groups are reduced in size during high security times. Fan discloses a firewall (i.e., access control system), wherein a group of cards (i.e., particular users; See col.8, line 20) changes as a function of time (See col.8, lines 19-21 and col. 9, lines 27-28), and said peer groups are reduced in size during high security times (See col.8, lines 21-24; i.e. wherein the fact that certain users cannot communicate outside the local area network during non-business hours implies that said group including said certain users (i.e. peer group) is reduced in size during non-business hours (i.e. high security times)). Therefore, it would have been obvious one of ordinary skill in the art at the time the invention was made to have included said access control system, as disclosed by Fan, in said modular switch, as disclosed by Porter, for the advantage of protecting a local area network using said modular switch from all uninvited sessions initiated externally (See Fan, col. 8, lines 13-15).

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Porter [WO 93/15464] in view of Ha-Duong [US 5,768,270 A].

Referring to claim 22, Porter discloses all the limitations of claim 22 except that does not teach a filter which passes to said card only data from said sub-buses to which said card listens. Ha-Duong discloses an ATM switch, wherein a filter for at least one of said cards which passes to said card only data from said sub-buses to which said card listens (See col. 6, lines 17-20; i.e. wherein the fact that a filter handles an input line of a concentrator in order to eliminate ATM cells which are not destined for its group of outputs implies that said filter for input line of concentrator (which is ultimately connected to at least one of said cards) passes to said card only ATM cells (i.e. data) from two-way lines (i.e. said sub-buses) to its group of outputs (i.e. to which said card listens)). Therefore, it would have been obvious one of ordinary skill in the art at the time the invention was made to have included said filter in said ATM switch, as disclosed by Ha-Duong, in said modular switch, as disclosed by Porter, for the advantage of outputting relevant ATM cells to said card (i.e. concentrator) (See Ha-Duong, col. 7, lines 4-5).

Claims 23-29 are rejected under 35 U.S.C. 102(b) as being anticipated by LaBerge [US 5,771,358 A].

Referring to claim 23, LaBerge discloses a method of allocating sub-buses (i.e., apportioning bus bandwidth; See col. 1, lines 6-8) to cards (i.e., bus requesters 26,28,30,32 of Fig. 1) of a switch (i.e., bus controller 24 of Fig. 1), comprising: determining bandwidth needs of each of said cards (See Fig. 3 and col. 5, lines 9-26); assigning each of said cards a bus demand value (i.e., weighting value) which is a function (See col. 3, lines 35-36) of said bandwidth needs of said card and a current bandwidth allocated to said card (See Fig. 2-3 and col. 3, lines 45+); and allocating (i.e., apportioning) said sub-buses (i.e., bus bandwidth) to said cards (i.e., bus requesters) based on said bus demand values of said cards (See col. 3, lines 36-44 and col. 4, lines 21-28).

Referring to claims 24-26, LaBerge discloses said method comprises 1) receiving messages (i.e., address strobes) from said cards, 2) determining a measure of utilization (See Fig. 3-4) of said sub-buses currently allocated to said card, and 3) listening (i.e., monitoring) to said sub-buses currently allocated to said card (See col. 5, 61-63). Refer to col. 5, lines 38-63.

Referring to claims 27-28, LaBerge discloses assigning a bus demand value (i.e., weighting value) which is a function of 1) a bandwidth requirement of said card (See col. 5, lines 58-61), and 2) a static maximum requester bandwidth which must be allocated to said card (See col. 5, line 67 through col. 6, line 8).

Referring to claim 29, LaBerge discloses allocating sub-buses not currently allocated to a specific card as additional sub-buses to said cards with the highest bus demand values (See col.4, lines 30-32 and lines 37-46).

Claims 31-33 and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Porter [WO 93/15464] in view of LaBerge [US 5,771,358 A].

Referring to claim 31, Porter discloses a modular switch (i.e., backplane 20 with line switches in Fig 2), comprising: a plurality of communication cards (i.e., boards; See page 1, lines 9-10 and page 3, lines 21+); a plurality of backplane sub-buses (i.e., bus lines 1-96 of Fig 4; See page 14, lines 20-23) each allocatable to one or more of said cards (i.e., a cluster of boards together; See page 4, lines 2-6); and at least one controller (i.e., switching circuits 26 and central processing unit 27 of Fig. 2) which is configurable to divide said cards into different numbers of groups (See Fig. 1 and page 14, line 22 through page 15, line 12 and page 15, line 28 through page 16, line 2), such that said cards of the different groups do not transmit data to each other (See page 15, lines 6-12 and line 25 through page 16, line 2; i.e., wherein in fact that the position of all the switches within the two sets is determined and therefore the relative conditions of interconnections between each of the slots and the bus is determined by such configuration implies that said cards of the different groups (i.e., different clusters) do not transmit data to each other (i.e., do not communicate)). Porter does not disclose said at least one controller is further configurable to allocate said sub-buses to said cards based on bus demand values of said cards. LaBerge discloses a system for apportioning computer bus bandwidth, wherein at least one controller (bus controller 24 of Fig. 1) is configurable to allocate (i.e. apportioning) said sub-buses (i.e. bus bandwidth) to said cards (i.e. bus requesters) based on bus demand values of said cards (See col. 3, lines 36-44 and col. 4, lines 21-28). Therefore, it would have been obvious one of ordinary skill in the art at the time the invention was made to have applied said bandwidth allocation method, as disclosed by LaBerge, to said modular switch, as disclosed by Porter, for the advantage of apportioning said bandwidth based on said bus demand value enables higher bandwidth cards to continue to operate at a relatively high bandwidth when said bus is saturated (See LaBerge, col. 6, lines 19-21).

Referring to claim 32, Porter teaches said at least one controller is configurable to divide said cards into any number of groups between one and said number of cards (See page 4, lines 2-6 and page 15, line 25 through page 16, line 2; i.e., wherein in fact that the invention gives massive flexibility to a

backplane and allows a wide number of different cluster configurations implies that switching circuits and processing unit (i.e., controller) is configurable to divide said slots into any number of groups between one and said number of slots).

Referring to claim 33, Porter teaches said number of groups are configured by a user (See page 15, lines 10-17; i.e., wherein in fact that after configuring, the condition of the interconnection remains unchanged, during normal operation until modification desired, and the condition of each switch can be determined during alteration implies that said number of groups (i.e., number of clusters) are configured (i.e., reconfigured) by a user (i.e., by alteration of programming instruction)).

Referring to claim 35, Porter teaches said cards of the different groups do not communicate (viz., do not transmit data to each other; See page 15, lines 6-12 and line 25 through page 16, line 2; i.e., wherein in fact that the position of all the switches within the two sets is determined and therefore the relative conditions of interconnections between each of the slots and the bus is determined by such configuration implies that said cards of the different groups (i.e., different clusters) do not communicate).

Referring to claim 36, Porter teaches said cards of the different groups do not communicate (viz., do not transmit data to each other) over any of said plurality of backplane sub-buses (See page 15, lines 6-12 and line 25 through page 16, line 2; i.e., wherein in fact that the position of all the switches within the two sets is determined and therefore the relative conditions of interconnections between each of the slots and the bus is determined by such configuration implies that said cards of the different groups (i.e., different clusters) do not communicate over any of said plurality of backplane sub-buses).

Referring to claim 37, Porter teaches a box (i.e., a computer backplane; See Fig. 2 and title) having a plurality of slots (i.e., slots 21 of Fig. 2) in which said cards (i.e., cards in said slots) are located. Porter, as modified by LaBerge, does not disclose wherein said cards of at least one group are not located in adjacent slots. The examiner takes official notice that said cards of one group are not located in adjacent slots (i.e. all said cards are inserted into non-adjacent slots) is well known in the art of backplane

bus configuration with a technology of programmatic switching circuitry. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to recognize said cards of one group are not located in adjacent slots since it would have allowed for greater flexibility to said cards being physically located at any slot in said box.

Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Porter [WO 93/15464] in view of LaBerge [US 5,771,358 A] as applied to claims 31-33 and 35-37 above, and further in view of AAPA.

Referring to claim 34, Porter discloses said at least one controller divides said cards into a number of groups. Porter, as modified by LaBerge, does not disclose said number of groups equal to a number of types of cards included in said plurality of cards. AAPA states it is desired to form separate connections using different protocols (i.e., different types of communication cards) without signal conversion by creating separate networks which are not interconnected (See page 2, lines 6-9; i.e., wherein in fact that said different types of communications cards forms said separate networks without said signal conversion implies that said number of separate networks (i.e. number of groups) equal to said different types of communications cards (i.e. number of types of cards) included in said plurality of communications cards (i.e. said plurality of cards)). Therefore, it would have been obvious one of ordinary skill in the art at the time the invention was made to have applied said grouping method, as disclosed by AAPA, to said switch, as disclosed by Porter, as modified by LaBerge, for the advantage of Ethernet and ATM can be interconnected without signal conversions (See AAPA, page 2, lines 7-8).

Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Porter [WO 93/15464] in view of LaBerge [US 5,771,358 A] as applied to claims 31-33 and 35-37 above, and further in view of Riley [US 5,875,351 A].

Referring to claim 38, Porter, as modified by LaBerge, discloses all the limitations of claim 38 except that does not teach only one card writes to a sub-bus at any single time. Riley discloses a

distributed DMA architecture, wherein only one card (i.e., network card 120 of Fig. 2) writes to a sub-bus (i.e., PCI bus 112 of Fig. 2) at any single time (See Fig. 8 and col. 19, lines 19-30). Therefore, it would have been obvious one of ordinary skill in the art at the time the invention was made to have included said distributed DMA architecture, as disclosed by Riley, in said switch, as disclosed by Porter, as modified by LaBerge, for the advantage of individual DMA channels can be distributed among said cards requiring DMA transfers, thereby supporting DMA on said sub-bus without requiring any change to existing software (See Riley, col. 4, line 65 through col. 5, line 2).

(11) Response to Argument

In response to the Appellants' argument with respect to "... The term 'sub-bus' as used in the claims is therefore clearly distinct from a slot or set of slots of a time domain multiplexed bus, in accordance with the explicit teachings of the specification. Applicants have in effect defined the term 'sub-bus' in their specification to exclude a slot or set of slots of a time domain multiplexes bus. ... The Examiner in the final Office Action at page 15, section 25, argues that cell slots of a time domain multiplexed bus such as that taught by Prince meet the 'plurality of backplane sub-buses' limitation of claim 1. Applicant submit that this interpretation is directly contrary to the explicit description of the term 'sub-bus' provided in the above-cited portion of the specification. ... The specification makes it abundantly clear that the term 'sub-bus' as used in the present application is distinct from a slot or set of slots of a time domain multiplexed bus. ..." in the Argument Section, pages 4-6 of the Appeal Brief filed on 21st of July, 2003 (hereinafter the Appeal Brief), the Examiner respectfully disagrees. In contrary to the Appellants' statement, the Appellants admit to define the term "sub-bus" to include a slot or set of slots of a time domain multiplexes bus (See the Appeal Brief, page 5, line 2), and in their specification, too (See Application, page 1, line 27). Accordingly, the term "sub-bus" as used in the claims is not clearly distinct from a slot or set of slots of a time domain multiplexed bus, in accordance with the explicit teachings of the specification. Therefore, the Examiner's interpretation of Prince in the final Office

Action at page 15, paragraph 25, such that cell slots of a time domain multiplexed bus meet the 'plurality of backplane sub-buses' limitation of claim 1, is within the scope of the Appellants' claimed invention. Furthermore, it is noted that the features upon which appellants rely (i.e., a plurality of backplane sub-buses, rather than a single time domain multiplexed bus) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Thus, Appellants' argument for this point cannot be seen as persuasive.

In response to the Appellants' argument with respect to "... Again, this arrangement involves a single physical bus without separately-identifiable sub-buses, whereas the present invention, as recited in independent claim 23, is directed to an arrangement involving a plurality of sub-buses. ..." in the Argument Section, Issue 3 of the Appeal Brief, the Examiner respectfully disagrees. In contrary to the Appellants' statement, it is noted that the features upon which appellants rely (i.e., a plurality of separately-identifiable sub-buses) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Thus, Appellants' argument for this point cannot be seen as persuasive.

In response to the Appellants' argument that the Examiner's conclusion of obviousness for the *35 USC §103(a)* rejection fails to establish a *prima facie* case of obviousness in the Argument Section of the Appeal Brief, the Examiner respectfully disagrees. In contrary to the Appellants' statement, all the rejections under *35 USC §103(a)* in the prior and the instant Examiner's Answer established a *prima facie* case of obviousness meeting the three basic criteria of the M.P.E.P. 2143.03 (8th ed. 2001). Furthermore, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to

one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the Examiner has clearly pointed out rationale for appropriate combination of the references. Thus, Appellants' argument for this point cannot be seen as persuasive.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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